READ ONLY MEMORY

20K Cartridge ROM

FEATURES

- Mask Programable Storage Providing 2048 x 10 Bit Words
- 16 Bit On-Chip Address Latch
- Memory Map Circuitry to Place the 2K ROM Page Within a 65K Memory Area
- 16 Bit Tri-State Bus with Higher 6 Bits Driven to Zero During Read Operations

CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1610 microprocessor. It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

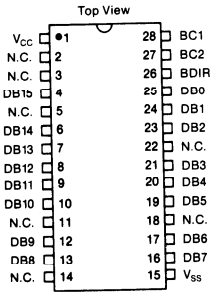
DESCRIPTION

From initialization, the RO-3-9504 waits for the first address code i.e., BAR. For this address code and all subsequent address sequences, the 9504 reads the 16-bit external bus and latches the value into its address register.

The 9504 contains a programable memory map location for its own 2K page, and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus.

PIN CONFIGURATION

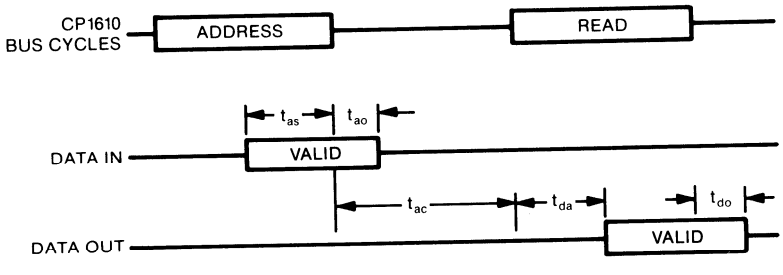
28 LEAD DUAL IN LINE



INPUT CONTROL SIGNALS

BDIR	BC1	BC2	Equivalent Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = High Impedance
0	0	1	IAB	No Action
0	1	0	ADAR	Address Data to Address Register, D0-D15 = High Impedance
0	1	1	DTB (READ)	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	No Action
1	1	0	DW	No Action
1	1	1	INTAK	INTerrupt AcKnowledge

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to 100°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

T_A = 0°C to +55°C
V_{CC} = +4.85V − +5.15V
V_{SS} = 0.0V

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
Input Logic Low	V_{IL}	0	0.7	V	
Input Logic High	V_{IH}	2.4	V_{CC}	V	
Input Leakage	V_{IL}	—	5	μA	V_{IN} = 0V to V_{CC}
Capacitance	—	—	10	pf	V_{IN} = 0V
CPU BUS Outputs					
Output Logic Low	V_{OL}	0	0.5	V	I_{OL} = 1.5mA +150pf
Output Logic High	V_{OH}	2.4	V_{CC}	V	I_{OH} = −200μA
Supply Current					
V_{CC} Supply	I_{CC}	—	120	mA	25°C

AC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
Address Set Up	t_{as}	400	—	ns	
Address Overlap	t_{ao}	65	—	ns	
CPU BUS Outputs					
Turn ON Delay	t_{da}	—	350	ns	
Turn OFF Delay	t_{do}	85	—	ns	
Access Time	t_{ac}	—	1.5	μs	